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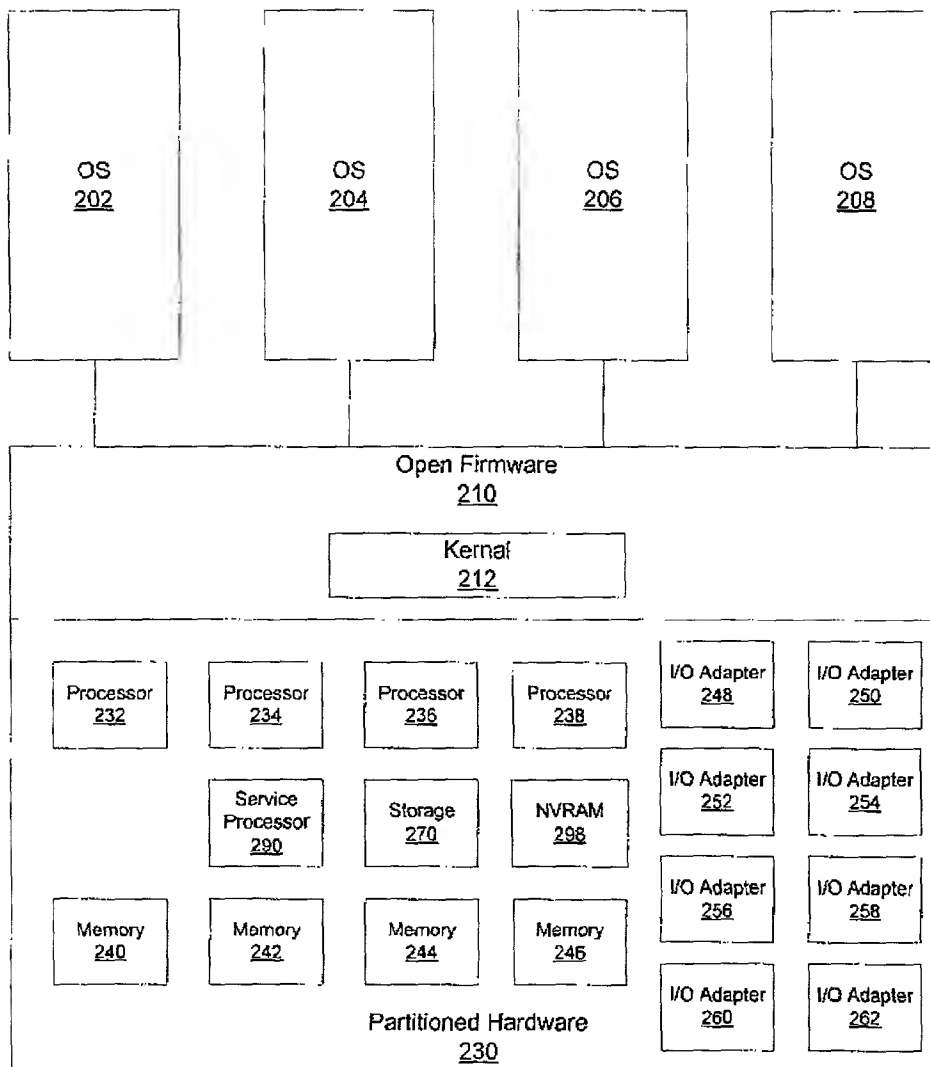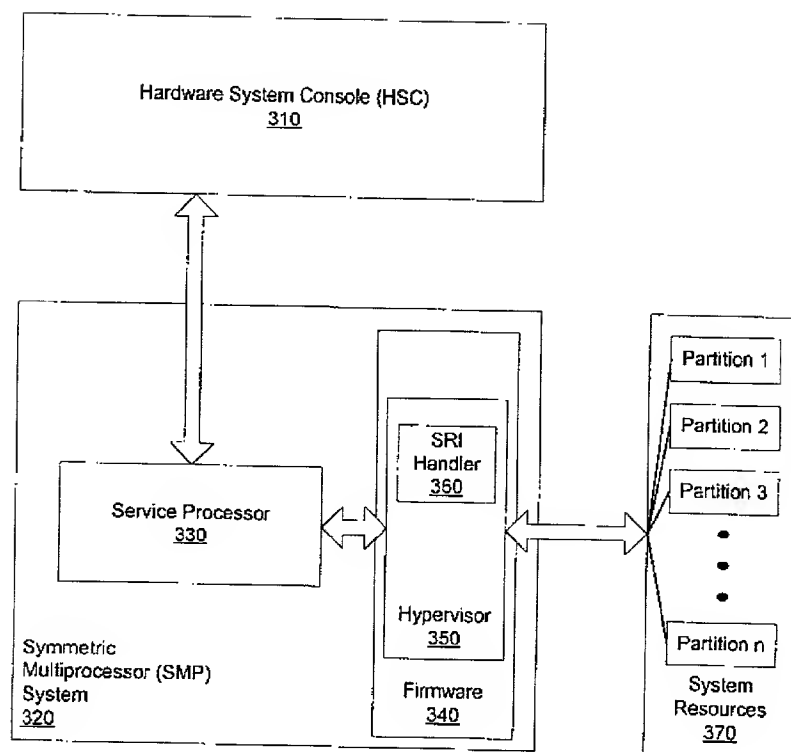Graphics Adapter 148

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Figure 1

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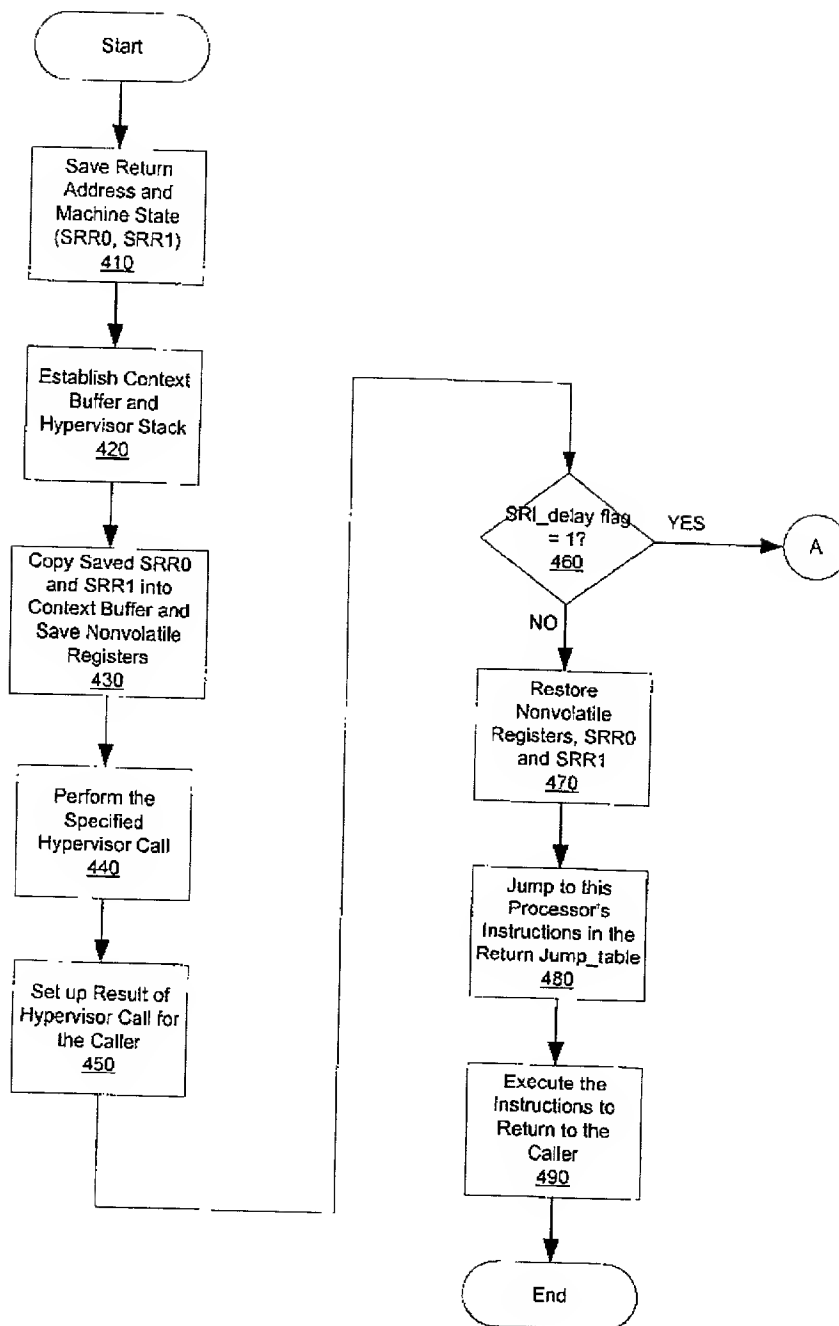230

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Figure 2

Figure 3

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Logical Partition Management
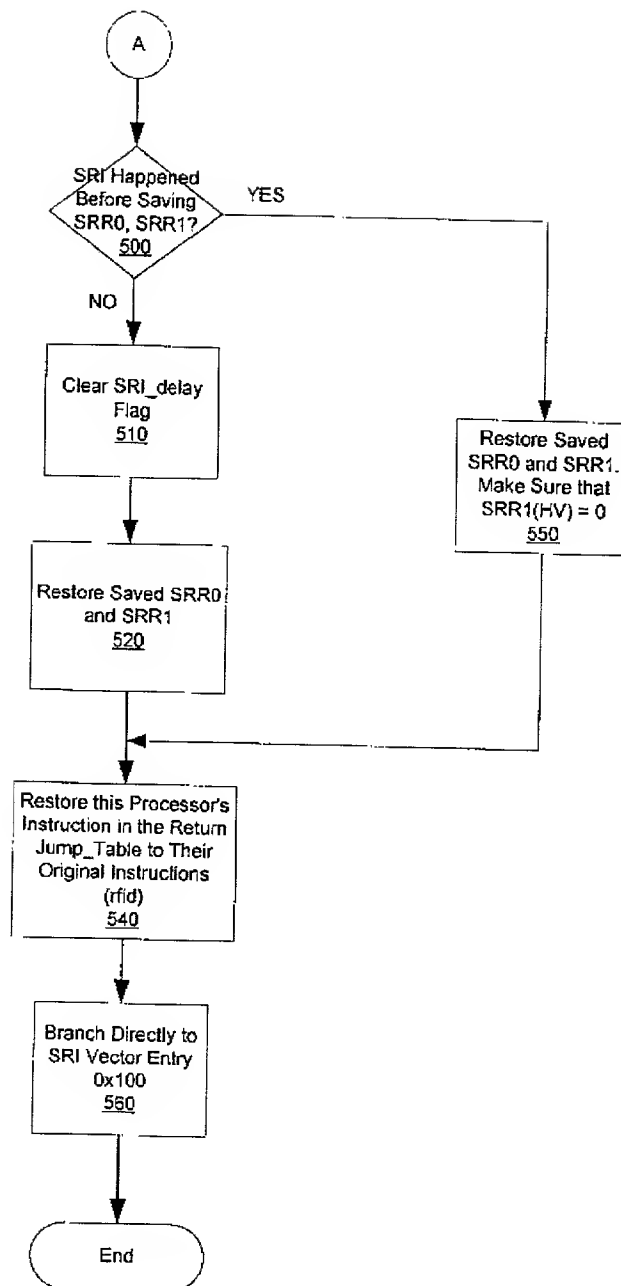Apparatus and Method for Handling
System Reset Interrupts
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```
                    ┌─────────┐
                    │  Start  │
                    └────┬────┘
                         │
                         ▼
              ┌──────────────────┐
              │   Save Return    │
              │   Address and    │
              │  Machine State   │
              │  (SRR0, SRR1)    │
              │       410        │
              └────────┬─────────┘
                       │
                       ▼
              ┌──────────────────┐
              │ Establish Context│
              │    Buffer and    │
              │ Hypervisor Stack │
              │       420        │
              └────────┬─────────┘
                       │
                       ▼
              ┌──────────────────┐
              │ Copy Saved SRR0  │
              │  and SRR1 into   │
              │ Context Buffer and│
              │ Save Nonvolatile │
              │    Registers     │
              │       430        │
              └────────┬─────────┘
                       │
                       ▼
              ┌──────────────────┐
              │   Perform the    │
              │    Specified     │
              │  Hypervisor Call │
              │       440        │
              └────────┬─────────┘
                       │
                       ▼
              ┌──────────────────┐
              │ Set up Result of │
              │ Hypervisor Call for│
              │    the Caller    │
              │       450        │
              └──────────────────┘
```

```
                    SRI_delay flag      YES      ┌───┐
                       = 1?          ──────────▶ │ A │
                        460                      └───┘
                        │ NO
                        ▼
              ┌──────────────────┐
              │     Restore      │
              │   Nonvolatile    │
              │ Registers, SRR0  │
              │    and SRR1      │
              │       470        │
              └────────┬─────────┘
                       │
                       ▼
              ┌──────────────────┐
              │  Jump to this    │
              │   Processor's    │
              │ Instructions in the│
              │ Return Jump_table│
              │       480        │
              └────────┬─────────┘
                       │
                       ▼
              ┌──────────────────┐
              │   Execute the    │
              │ Instructions to  │
              │  Return to the   │
              │     Caller       │
              │       490        │
              └────────┬─────────┘
                       │
                       ▼
                  ┌─────────┐
                  │   End   │
                  └─────────┘
```

Figure 4

Figure 5

```
                        ┌──────────┐
                        │  Start   │
                        └────┬─────┘
                             │
                             ▼
                   ┌──────────────────┐
                   │ Execution Starts at│         ╱◇╲
                   │  SRI Vector Entry  │      SRI Occurred
                   │      0x100         │        Inside        NO      ┌───┐
                   │       610          │       Hypervisor?  ─────────▶│ B │
                   └─────────┬──────────┘          660               └───┘
                             │                      ╲◇╱
                             ▼                       │ YES
                   ┌──────────────────┐              ▼
                   │  Save Register    │   ┌──────────────────┐
                   │ Context to Memory │   │ Set SRI_Delay flag │
                   │     Buffer        │   │       670          │
                   │       620         │   └─────────┬──────────┘
                   └─────────┬─────────┘             │
                             │                        ▼
                             ▼             ┌────────────────────┐
                          ╱◇╲              │ Change Processor's  │
                       Hard Reset?   NO    │ Jump_Table Instruction│
                          630     ─────┐   │ to a Branch Instruction│
                          ╲◇╱          │   │ to Simulated SRI Entry │
                           │ YES       │   │      Point          │
                           ▼           │   │       680           │
                   ┌──────────────┐    │   └─────────┬───────────┘
                   │ Clear SRI_Delay│   │             │
                   │   Flag to 0    │   │             ▼
                   │     640        │   │   ┌──────────────────┐
                   └───────┬────────┘   │   │ Restore Register  │
                           │            │   │    Context and    │
                           ▼            │   │    Return to      │
                   ┌──────────────┐     │   │   Interrupted     │
                   │ Send Processor│    │   │  Hypervisor Call  │
                   │ Back to Global│    │   │      690          │
                   │  Available    │    │   └─────────┬─────────┘
                   │ Processor Pool│    │             │
                   │     650       │    │             │
                   └───────┬───────┘    │             │
                           │            │             │
                           ▼            │             │
                        ┌──────────┐◀───┘◀────────────┘
                        │   End    │
                        └──────────┘
```

Figure 6

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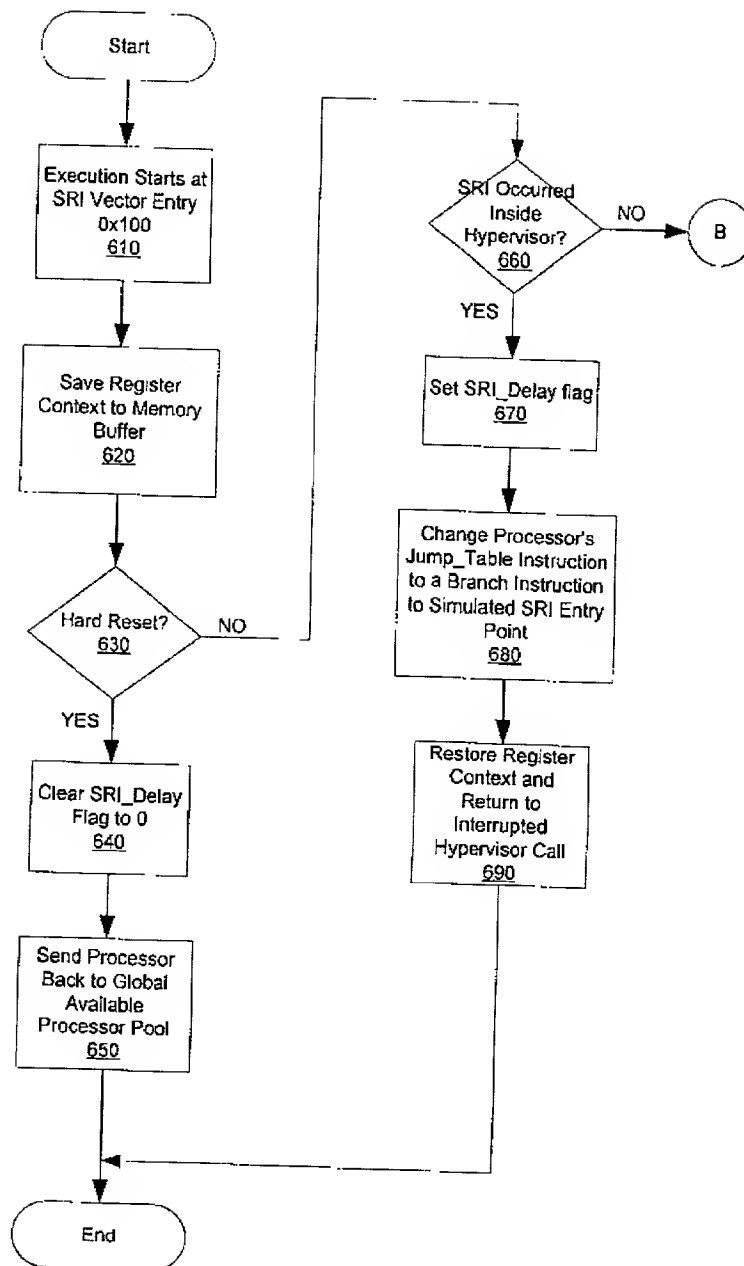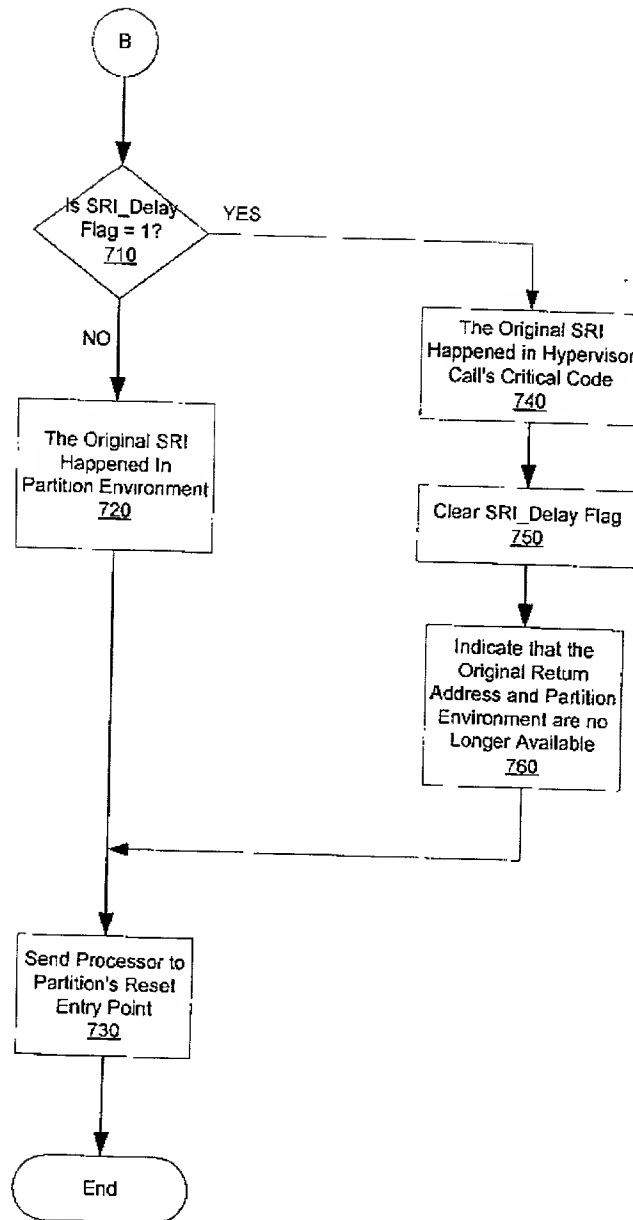Apparatus and Method for Handling
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B

Is SRI_Delay
Flag = 1?
710

YES

NO

The Original SRI
Happened in Hypervisor
Call's Critical Code
740

The Original SRI
Happened In
Partition Environment
720

Clear SRI_Delay Flag
750

Indicate that the
Original Return
Address and Partition
Environment are no
Longer Available
760

Send Processor to
Partition's Reset
Entry Point
730

End

Figure 7

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